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CHEN, QING	
ART UNIT	**PAPER NUMBER**
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SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/734,457	JOHNSON ET AL.	
	Examiner	Art Unit	
	Qing Chen	2191	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☒ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____.

DETAILED ACTION

1. This is the initial Office action based on the application filed on December 12, 2003.

2. **Claims 1-29** are pending.

Oath/Declaration

3. The oath or declaration is defective. A new oath or declaration in compliance with 37 CFR 1.67(a) identifying this application by application number and filing date is required. See MPEP §§ 602.01 and 602.02.

The oath or declaration is defective because:
It does not state that the person making the oath or declaration believes the named inventor or inventors to be the first inventor or inventors of the subject matter which is claimed and for which a patent is sought.

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description:

- Reference number "305b" in Figure 4B.
- Reference number "328" in Figure 5.

Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application.

5. The drawings are objected to because the specification discloses that some drawing elements of Figure 1A are shown as shaded area *(see Page 3, Paragraph [0013])*. However,

Figure 1A does not include any shaded drawing elements. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application.

Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the Examiner, the Applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

6. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

7. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed

150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

8. The abstract of the disclosure is objected to because:

- It contains phrases which can be implied, such as "In general, in one aspect, the disclosure describes ..."
- It contains the following typographical errors:
  - The phrase "instructions that relinquishes ..." should read "instructions that relinquish ..."
  - The phrase "another thread will be concurrently ..." should read "another thread that will be concurrently ..."
  - The term "processor" should read "multi-tasking processor."

Correction is required. See MPEP § 608.01(b).

9. The use of trademarks, such as INTEL, has been noted in this application. Trademarks should be capitalized wherever they appear (capitalize each letter OR accompany each trademark with an appropriate designation symbol, *e.g.*, ™ or ®) and be accompanied by the generic terminology (use trademarks as adjectives modifying a descriptive noun, *e.g.*, "the JAVA programming language").

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner, which might adversely affect their validity as trademarks.

Claim Objections

10. **Claims 1-18, 20-23, 25, and 29** are objected to because of the following informalities:

- **Claims 1, 2, 4-10, 12-18, 20, and 21** recite the limitation "the processor." Applicant is advised to change this limitation to read "the multi-tasking processor" for the purpose of providing it with proper explicit antecedent basis.
- **Claim 3** depends on Claim 2 and, therefore, suffers the same deficiency as Claim 2.
- **Claim 11** depends on Claim 10 and, therefore, suffers the same deficiency as Claim 10.
- **Claims 22 and 23** depend on Claim 21 and, therefore, suffer the same deficiency as Claim 21.
- **Claims 7 and 18** contain a typographical error: the phrase "a number of consecutive instructions ending a one of the nodes" should presumably read "a number of consecutive instructions ending at one of the nodes."
- **Claim 18** contains a typographical error: Claim 18 should depend on Claim 12, not Claim 1.
- **Claim 25** recites the limitation "the threads." Applicant is advised to change this limitation to read "the multiple threads" for the purpose of providing it with proper explicit antecedent basis.

- **Claim 29** contains a typographical error: the word "a" should be deleted in the phrase "wherein the multi-tasking processor comprises a one of a set of multi-tasking processors …"

Appropriate correction is required.

Claim Rejections - 35 USC § 112

11. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

12. **Claims 11-29** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 11 and 22 recite the limitation "the engine." There is insufficient antecedent basis for this limitation in the claims. In the interest of compact prosecution, the Examiner subsequently interprets this limitation as reading "the multi-threaded engine" for the purpose of further examination.

Claim 23 depends on Claim 22 and, therefore, suffers the same deficiency as Claim 22.

Claims 12-23 recite the limitation "the program." There is insufficient antecedent basis for this limitation in the claims. In the interest of compact prosecution, the Examiner

subsequently interprets this limitation as reading "the computer program product" for the purpose of further examination.

Claim 24 recites the limitation "at least some." The term "some" is a relative term, which renders the claim indefinite. The term "some" is not defined by the claim nor does the specification provide a standard for ascertaining the requisite degree and one of ordinary skill in the art would not be able to reasonably determine the scope of the invention. In the interest of compact prosecution, the Examiner subsequently does not give any patentable weight to this limitation for the purpose of further examination.

Claims 25-29 depend on Claim 24 and, therefore, suffer the same deficiency as Claim 24.

Claim 25 recites the limitation "a more equal." The term "more" is a relative term, which renders the claim indefinite. The term "more" is not defined by the claim nor does the specification provide a standard for ascertaining the requisite degree and one of ordinary skill in the art would not be able to reasonably determine the scope of the invention. In the interest of compact prosecution, the Examiner subsequently does not give any patentable weight to this limitation for the purpose of further examination.

Claim 26 recites the limitation "a greater share." The term "greater" is a relative term, which renders the claim indefinite. The term "greater" is not defined by the claim nor does the

specification provide a standard for ascertaining the requisite degree and one of ordinary skill in the art would not be able to reasonably determine the scope of the invention. In the interest of compact prosecution, the Examiner subsequently does not give any patentable weight to this limitation for the purpose of further examination.

Claim 29 recites the limitation "the same semiconductor chip." There is insufficient antecedent basis for this limitation in the claim. In the interest of compact prosecution, the Examiner subsequently interprets this limitation as reading "a semiconductor chip" for the purpose of further examination.

Claim Rejections - 35 USC § 101

13. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

14. **Claims 12-29** are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 12-23 recite computer readable medium as a claimed element. However, the claims recite a computer program product being <u>disposed</u> (emphasis added) on the computer readable medium, which does not suggest that the computer program product is being recorded on the computer readable medium. Consequently, the computer readable medium can be

reasonably interpreted as carrying electrical signals, since the computer program product is not tangibly embodied (stored) on the computer readable medium.

Claims that recite nothing but the physical characteristics of a form of energy, such as a frequency, voltage, or the strength of a magnetic field, define energy or magnetism *per se*, and as such are nonstatutory natural phenomena. *O'Reilly v. Morse*, 56 U.S. (15 How.) 62, 112-14 (1853). Moreover, it does not appear that a claim reciting a signal encoded with functional descriptive material falls within any of the categories of patentable subject matter set forth in § 101.

The result of **Claims 24-29** is directed to the act of "managing execution control," which does not appear to be a tangible result so as to constitute a practical application of the idea. The act of "managing execution control" is merely a thought or an abstract idea and does not appear to produce a tangible result even if the step of management does occur, since the result of that management is not conveyed in the real world. The result is a management, which is neither used in a disclosed practical application nor made available for use in a disclosed practical application. It also does not appear that the usefulness of the management can be realized from the claimed steps to support a disclosed specific, substantial, and credible utility so as to produce a useful result.

Therefore, the claims do not meet the statutory requirement of 35 U.S.C. § 101, since the claims are not directed to a practical application of the § 101 judicial exception producing a result tied to the physical world.

Claim Rejections - 35 USC § 102

15. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

16. **Claims 1-4, 7-15, 18-27, and 29** are rejected under 35 U.S.C. 102(b) as being anticipated by **Dubey et al. (US 5,812,811)**.

As per **Claim 1**, Dubey et al. disclose:

- automatically inserting into instructions of a first thread at least one instruction that relinquishes control of a multi-tasking processor to another thread that will be concurrently sharing the multi-tasking processor *(see Column 16: 23-42, "An UNCOND_SUSPEND instruction is inserted at the end of every future thread." and "Upon encountering an UNCOND_SUSPEND instruction, during its corresponding future thread execution, a future thread unconditionally suspends itself." and "If an UNCOND_SUSPEND instruction is encountered for execution by a thread other than its corresponding future thread (e.g., in the main thread), it is ignored.").*

As per **Claim 2**, the rejection of **Claim 1** is incorporated; and Dubey et al. further disclose:

- automatically inserting into instructions of a second thread at least one instruction that relinquishes control of the multi-tasking processor to another thread that will be concurrently sharing the multi-tasking processor *(see Column 16: 23-42, "An UNCOND_SUSPEND instruction is inserted at the end of every future thread." and "Upon encountering an UNCOND_SUSPEND instruction, during its corresponding future thread execution, a future thread unconditionally suspends itself." and "If an UNCOND_SUSPEND instruction is encountered for execution by a thread other than its corresponding future thread (e.g., in the main thread), it is ignored.").*

As per **Claim 3**, the rejection of **Claim 2** is incorporated; and Dubey et al. further disclose:

- automatically inserting into instructions of the first thread comprises inserting based on at least one characteristic of the instructions of the second thread *(see Column 14: 57-61, "The identification of fork points involves data and control dependence analysis, based on some or all of the corresponding program dependence graph (combination of control dependence graph and data dependence graph), using techniques known in the prior art.")*; and
- automatically inserting into instructions of the second thread comprises inserting based on at least one characteristic of the instructions of the first thread *(see Column 14: 57-61, "The identification of fork points involves data and control dependence analysis, based on some or all of the corresponding program dependence graph (combination of control dependence graph and data dependence graph), using techniques known in the prior art.").*

As per **Claim 4**, the rejection of **Claim 2** is incorporated; and Dubey et al. further disclose:

- repeating a procedure that determines one or more locations to automatically insert instructions that relinquish control of the multi-tasking processor into the instructions of the first and second threads *(see Column 14: 57-61, "The identification of fork points involves data and control dependence analysis, based on some or all of the corresponding program dependence graph (combination of control dependence graph and data dependence graph), using techniques known in the prior art.")*.

As per **Claim 7**, the rejection of **Claim 1** is incorporated; and Dubey et al. further disclose:

- constructing a data flow graph of the instructions of the first thread, the data flow graph comprising an organization of nodes associated with subsets of the instructions of the first thread *(see Figures 5A, 5B, and 6; Column 21: 29-30, "... different control independent blocks, such as, B1 and B12, in FIG. 5.")*; and
- determining at least one of the following:
  - a number of consecutive instructions ending at one of the nodes that do not relinquish control of the multi-tasking processor;
  - a number of consecutive instructions beginning at one of the nodes that do not relinquish control of the multi-tasking processor; and
  - a number of consecutive instructions between instructions of one of the nodes that relinquish control of the multi-tasking processor *(see Column 21: 45-47, "Conditional suspend,*

or, SUSPEND instruction is used in block B9 to speculatively execute next two instructions ... " and 52-53, "... SUSPEND instruction is used to speculatively execute next four instructions. ").

As per **Claim 8**, the rejection of **Claim 1** is incorporated; and Dubey et al. further disclose:

- wherein automatically inserting comprises inserting to keep intact a group of instructions identified as indivisible *(see Column 21: 14-16, "Code sequences shown have been broken into blocks of non-branch instructions, optionally ending with a branch instruction. ").*

As per **Claim 9**, the rejection of **Claim 1** is incorporated; and Dubey et al. further disclose:

- wherein the multi-tasking processor comprises a multi-threaded central processor unit (CPU) *(see Column 4: 51-53, "The present invention is an enhancement to a central processing unit (CPU) in a computer that permits speculative parallel execution of more than one instruction thread. ").*

As per **Claim 10**, the rejection of **Claim 1** is incorporated; and Dubey et al. further disclose:

- wherein the multi-tasking processor comprises a multi-threaded engine of a multi-engine processor *(see Column 4: 51-53, "The present invention is an enhancement to a central processing unit (CPU) in a computer that permits speculative parallel execution of more than one instruction thread. ").*

As per **Claim 11**, the rejection of **Claim 10** is incorporated; and Dubey et al. further disclose:

- wherein the multi-threaded engine of the multi-engine processor comprises an engine not having any floating point instructions in the multi-threaded engine's instruction set *(see Column 21: 16-19, "... the PowerPC architecture.")*.

As per **Claim 12**, Dubey et al. disclose:

- access instructions of a first thread *(see Column 14: 51-52, "Analyze this sequence of instructions to determine a set of fork points.")*; and

- insert into the instructions of a first thread at least one instruction that relinquishes control of a multi-tasking processor to another thread that will be concurrently sharing the multi-tasking processor *(see Column 16: 23-42, "An UNCOND_SUSPEND instruction is inserted at the end of every future thread." and "Upon encountering an UNCOND_SUSPEND instruction, during its corresponding future thread execution, a future thread unconditionally suspends itself." and "If an UNCOND_SUSPEND instruction is encountered for execution by a thread other than its corresponding future thread (e.g., in the main thread), it is ignored.")*.

As per **Claim 13**, the rejection of **Claim 12** is incorporated; and Dubey et al. further disclose:

- insert into instructions of a second thread at least one instruction that relinquishes control of the multi-tasking processor *(see Column 16: 23-42, "An UNCOND_SUSPEND*

instruction is inserted at the end of every future thread." and "Upon encountering an UNCOND_SUSPEND instruction, during its corresponding future thread execution, a future thread unconditionally suspends itself." and "If an UNCOND_SUSPEND instruction is encountered for execution by a thread other than its corresponding future thread (e.g., in the main thread), it is ignored.").

As per **Claim 14**, the rejection of **Claim 13** is incorporated; and Dubey et al. further disclose:

- insert into instructions of the first thread comprises inserting based on at least one characteristic of the instructions of the second thread *(see Column 14: 57-61, "The identification of fork points involves data and control dependence analysis, based on some or all of the corresponding program dependence graph (combination of control dependence graph and data dependence graph), using techniques known in the prior art.")*; and
- insert into instructions of the second thread comprises inserting based on at least one characteristic of the instructions of the first thread *(see Column 14: 57-61, "The identification of fork points involves data and control dependence analysis, based on some or all of the corresponding program dependence graph (combination of control dependence graph and data dependence graph), using techniques known in the prior art.").*

As per **Claim 15**, the rejection of **Claim 13** is incorporated; and Dubey et al. further disclose:

- repeat a procedure that determines one or more locations to automatically insert instructions that relinquish control of the multi-tasking processor into the instructions of the first and second threads *(see Column 14: 57-61, "The identification of fork points involves data and control dependence analysis, based on some or all of the corresponding program dependence graph (combination of control dependence graph and data dependence graph), using techniques known in the prior art.")*.

As per **Claim 18**, the rejection of **Claim 12** is incorporated; and Dubey et al. further disclose:

- construct a data flow graph of the instructions of the first thread, the data flow graph comprising an organization of nodes associated with subsets of the instructions of the first thread *(see Figures 5A, 5B, and 6; Column 21: 29-30, "... different control independent blocks, such as, B1 and B12, in FIG. 5.")*; and

- determine at least one of the following:

  - a number of consecutive instructions ending at one of the nodes that do not relinquish control of the multi-tasking processor;

  - a number of consecutive instructions beginning at one of the nodes that do not relinquish control of the multi-tasking processor; and

  - a number of consecutive instructions between instructions of one of the nodes that relinquish control of the multi-tasking processor *(see Column 21: 45-47, "Conditional suspend, or, SUSPEND instruction is used in block B9 to speculatively execute next two instructions ..." and 52-53, "... SUSPEND instruction is used to speculatively execute next four instructions.")*.

As per **Claim 19**, the rejection of **Claim 12** is incorporated; and Dubey et al. further disclose:

- wherein the instructions to insert comprise instructions to insert to keep intact a group of instructions identified as indivisible *(see Column 21: 14-16, "Code sequences shown have been broken into blocks of non-branch instructions, optionally ending with a branch instruction.")*.

As per **Claim 20**, the rejection of **Claim 12** is incorporated; and Dubey et al. further disclose:

- wherein the multi-tasking processor comprises a multi-threaded central processor unit (CPU) *(see Column 4: 51-53, "The present invention is an enhancement to a central processing unit (CPU) in a computer that permits speculative parallel execution of more than one instruction thread.")*.

As per **Claim 21**, the rejection of **Claim 12** is incorporated; and Dubey et al. further disclose:

- wherein the multi-tasking processor comprises a multi-threaded engine of a multi-engine processor *(see Column 4: 51-53, "The present invention is an enhancement to a central processing unit (CPU) in a computer that permits speculative parallel execution of more than one instruction thread.")*.

As per **Claim 22**, the rejection of **Claim 21** is incorporated; and Dubey et al. further disclose:

- wherein the multi-threaded engine of the multi-engine processor comprises an engine not having any floating point instructions in the multi-threaded engine's instruction set *(see Column 21: 16-19, "... the PowerPC architecture.")*.

As per **Claim 23**, the rejection of **Claim 22** is incorporated; and Dubey et al. further disclose:

- wherein the computer program product comprises at least one of the following: a compiler, an assembler, and a source code pre-processor *(see Column 4: 57-58, "... a compiler.")*.

As per **Claim 24**, Dubey et al. disclose:

- managing execution control of a multi-tasking processor shared by multiple threads by automatically inserting instructions into at least some of the multiple threads to relinquish control of the multi-tasking processor to a different thread *(see Column 16: 23-42, "An UNCOND_SUSPEND instruction is inserted at the end of every future thread." and "Upon encountering an UNCOND_SUSPEND instruction, during its corresponding future thread execution, a future thread unconditionally suspends itself." and "If an UNCOND_SUSPEND instruction is encountered for execution by a thread other than its corresponding future thread (e.g., in the main thread), it is ignored.")*.

As per **Claim 25**, the rejection of **Claim 24** is incorporated; and Dubey et al. further disclose:

- wherein managing comprises inserting instructions into the multiple threads to provide a more equal distribution of processor execution control among at least some of the threads than before the inserting *(see Column 4: 51-57, "The present invention is an enhancement to a central processing unit (CPU) in a computer that permits speculative parallel execution of more than one instruction thread. The invention discloses novel Fork-Suspend instructions that are added to the instruction set of the CPU, and are inserted in a program prior to run-time to delineate potential future threads for parallel execution.")*.

As per **Claim 26**, the rejection of **Claim 24** is incorporated; and Dubey et al. further disclose:

- wherein managing comprises inserting instructions into the threads to provide a subset of the multiple threads a greater share of processor execution control than before the inserting *(see Column 4: 51-57, "The present invention is an enhancement to a central processing unit (CPU) in a computer that permits speculative parallel execution of more than one instruction thread. The invention discloses novel Fork-Suspend instructions that are added to the instruction set of the CPU, and are inserted in a program prior to run-time to delineate potential future threads for parallel execution.")*.

As per **Claim 27**, the rejection of **Claim 24** is incorporated; and Dubey et al. further disclose:

- wherein the inserting comprises inserting based on data flow graphs generated for the, respective, threads *(see Figures 5A, 5B, and 6; Column 21: 29-30, "... different control independent blocks, such as, B1 and B12, in FIG. 5.")*.

As per **Claim 29**, the rejection of **Claim 24** is incorporated; and Dubey et al. further disclose:

- wherein the multi-tasking processor comprises one of a set of multi-tasking processors integrated on a semiconductor chip *(see Column 4: 51-53, "The present invention is an enhancement to a central processing unit (CPU) in a computer that permits speculative parallel execution of more than one instruction thread.")*.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. **Claims 5, 6, 16, and 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Dubey et al. (US 5,812,811)** in view of **Chrysos et al. (US 5,809,450)**.

As per **Claim 5**, the rejection of **Claim 3** is incorporated; however, Dubey et al. do not disclose:

- wherein the at least one characteristic of the instructions of the first thread comprises an average number of consecutive instructions that do not relinquish control of the multi-tasking processor.

Chrysos et al. disclose:

- wherein the at least one characteristic of the instructions of the first thread comprises an average number of consecutive instructions that do not relinquish control of the multi-tasking processor *(see Column 18: 19-22, "... function 755 takes as input state information 756 such as addresses, process identifiers, address space numbers, hardware context identifiers, or thread identifiers of the selected instructions." and 30-34, "Step 760 produces a subset of samples based on the function 755. In step 780, statistics 790 are determined. These statistics can include averages, standard deviations, histograms (distribution), and error bounds of the properties of the sampled instructions.").*

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Chrysos et al. into the teaching of Dubey et al. to include wherein the at least one characteristic of the instructions of the first thread comprises an average number of consecutive instructions that do not relinquish control of the multi-tasking processor. The modification would be obvious because one of ordinary skill in the art would be motivated to show the distribution of instruction execution, memory access rates, or latencies *(see Chrysos et al. – Column 18: 38-39).*

As per **Claim 6**, the rejection of **Claim 5** is incorporated; however, Dubey et al. do not disclose:

- wherein the at least one characteristic of the instructions of the first thread comprises a standard deviation derived from the number of consecutive instructions that do not relinquish control of the multi-tasking processor.

Chrysos et al. disclose:

- wherein the at least one characteristic of the instructions of the first thread comprises a standard deviation derived from the number of consecutive instructions that do not relinquish control of the multi-tasking processor *(see Column 18: 19-22, "... function 755 takes as input state information 756 such as addresses, process identifiers, address space numbers, hardware context identifiers, or thread identifiers of the selected instructions." and 30-34, "Step 760 produces a subset of samples based on the function 755. In step 780, statistics 790 are determined. These statistics can include averages, standard deviations, histograms (distribution), and error bounds of the properties of the sampled instructions.").*

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Chrysos et al. into the teaching of Dubey et al. to include wherein the at least one characteristic of the instructions of the first thread comprises a standard deviation derived from the number of consecutive instructions that do not relinquish control of the multi-tasking processor. The modification would be obvious because one of ordinary skill in the art would be motivated to show the distribution of instruction execution, memory access rates, or latencies *(see Chrysos et al. – Column 18: 38-39).*

As per **Claim 16**, the rejection of **Claim 14** is incorporated; however, Dubey et al. do not disclose:

- wherein the at least one characteristic of the instructions of the first thread comprises an average number of consecutive instructions that do not relinquish control of the multi-tasking processor.

Chrysos et al. disclose:

- wherein the at least one characteristic of the instructions of the first thread comprises an average number of consecutive instructions that do not relinquish control of the multi-tasking processor *(see Column 18: 19-22, "... function 755 takes as input state information 756 such as addresses, process identifiers, address space numbers, hardware context identifiers, or thread identifiers of the selected instructions." and 30-34, "Step 760 produces a subset of samples based on the function 755. In step 780, statistics 790 are determined. These statistics can include averages, standard deviations, histograms (distribution), and error bounds of the properties of the sampled instructions.")*.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Chrysos et al. into the teaching of Dubey et al. to include wherein the at least one characteristic of the instructions of the first thread comprises an average number of consecutive instructions that do not relinquish control of the multi-tasking processor. The modification would be obvious because one of ordinary skill in the art would be motivated to show the distribution of instruction execution, memory access rates, or latencies *(see Chrysos et al. – Column 18: 38-39)*.

As per **Claim 17**, the rejection of **Claim 16** is incorporated; however, Dubey et al. do not disclose:

- wherein the at least one characteristic of the instructions of the first thread comprises a standard deviation derived from the number of consecutive instructions that do not relinquish control of the multi-tasking processor.

<u>Chrysos et al.</u> disclose:

- wherein the at least one characteristic of the instructions of the first thread comprises a standard deviation derived from the number of consecutive instructions that do not relinquish control of the multi-tasking processor *(see Column 18: 19-22, "... function 755 takes as input state information 756 such as addresses, process identifiers, address space numbers, hardware context identifiers, or thread identifiers of the selected instructions." and 30-34, "Step 760 produces a subset of samples based on the function 755. In step 780, statistics 790 are determined. These statistics can include averages, standard deviations, histograms (distribution), and error bounds of the properties of the sampled instructions.")*.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of <u>Chrysos et al.</u> into the teaching of <u>Dubey et al.</u> to include wherein the at least one characteristic of the instructions of the first thread comprises a standard deviation derived from the number of consecutive instructions that do not relinquish control of the multi-tasking processor. The modification would be obvious because one of ordinary skill in the art would be motivated to show the distribution of instruction execution, memory access rates, or latencies *(see <u>Chrysos et al.</u> – Column 18: 38-39)*.

19. **Claim 28** is rejected under 35 U.S.C. 103(a) as being unpatentable over **<u>Dubey et al.</u> (US 5,812,811)** in view of **<u>Russell et al.</u> (US 5,680,645)**.

As per **Claim 28**, the rejection of **Claim 24** is incorporated; however, Dubey et al. do not disclose:

- wherein the multi-tasking processor comprises a co-operative multi-tasking processor.

Russell et al. disclose:

- wherein the multi-tasking processor comprises a co-operative multi-tasking processor *(see Column 12: 49-53, "A non-preemptive (cooperative multi-tasking) approach is used to divide the processor between the various application modules that are loaded ... ").*

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teaching of Russell et al. into the teaching of Dubey et al. to include wherein the multi-tasking processor comprises a co-operative multi-tasking processor. The modification would be obvious because one of ordinary skill in the art would be motivated to prevent one application module from preempting other modules by capturing the microprocessor *(see Russell et al. – Column 12: 52-53).*

Conclusion

20. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

A. **Borkenhagen et al. (US 6,212,544)** disclose an improved high performance multithreaded computer data processing system and method embodied in the hardware of the processor.

B. **<u>Alverson et al.</u> (US 6,480,818)** disclose a system for debugging targets using various techniques, some of which are particularly useful in a multithread environment.

C. **<u>Kalafatis et al.</u> (US 6,535,905)** disclose a method and apparatus for performing context (or thread) switching within a multithreaded processor.

D. **<u>Cota-Robles</u> (US 6,658,447)** discloses systems and methods for selecting instructions for execution in simultaneous multi-threaded processors.

E. **<u>Davis et al.</u> (US 6,931,641)** disclose computer systems in which the computer executes multiple threads of instruction so as to minimize the impact of latency in accessing data especially data formatted in tree structures.

F. **<u>D'Souza</u> (US 6,948,172)** discloses scheduling of tasks in data processing systems.

G. **<u>Shoemaker</u> (US 7,134,002)** discloses reducing idle time in simultaneous multi-threading processors with minimal circuit impact and minimal machine cost.

H. **<u>Ohsawa et al.</u> (US 7,134,124)** disclose a parallel processor system for dividing a single program into a plurality of threads and executing the above program in parallel by a plurality of processors.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Qing Chen whose telephone number is 571-270-1071. The Examiner can normally be reached on Monday through Thursday from 7:30 AM to 4:00 PM. The Examiner can also be reached on alternate Fridays.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Wei Zhen, can be reached on 571-272-3708. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the TC 2100 Group receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

QC / QC
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